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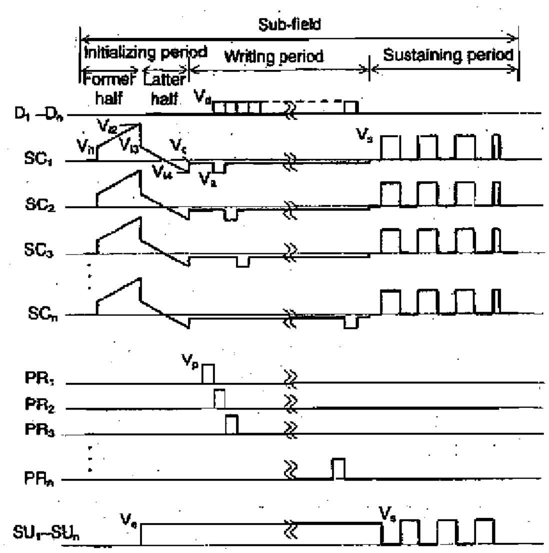
(54) **DRIVE METHOD FOR PLASMA DISPLAY PANEL**

(57) A method of driving a plasma display panel including priming electrodes (PR_1 to PR_n). In the writing period of a sub-field, prior to scanning of respective scan electrodes (SC_1 to SC_n), priming discharge is caused between the scan electrodes (SC_1 to SC_n) and the priming electrodes (PR_1 to PR_n). The time interval between the application of voltage to the priming electrodes (PR_1 to PR_n) for causing the priming discharge and the scanning of the corresponding scan electrodes (SC_1 to SC_n) is set within 10 μs.

FIG. 4



Description

TECNICAL FIELD

[0001] The present invention relates to a method of driving an alternating-current (AC) type plasma display panel.

BACKGROUND ART

[0002] A plasma display panel (hereinafter abbreviated as a PDP or a panel) is a display device having excellent visibility and featuring a large screen, thinness and light weight. The systems of discharging a PDP include an AC type and direct-current (DC) type. The electrode structures thereof include a three-electrode surface-discharge type and an opposite-discharge type. However, the current mainstream is an AC type three-electrode PDP, which is an AC surface-discharge type, because this type of PDP is suitable for higher definition and easy to manufacture.

[0003] Generally, an AC type three-electrode PDP has a large number of discharge cells formed between a front panel and rear panel faced with each other. In the front panel, a plurality of display electrodes, each made of a pair of scan electrode and sustain electrode, are formed on a front glass substrate in parallel with each other. A dielectric layer and a protective layer are formed to cover these display electrodes. In the rear panel, a plurality of parallel data electrodes is formed on a rear glass substrate. A dielectric layer is formed on the data electrodes to cover them. Further, a plurality of barrier ribs is formed on the dielectric layer in parallel with the data electrodes. Phosphor layers are formed on the surface of the dielectric layer and the side faces of the barrier ribs. Then, the front panel and the rear panel are faced with each other and sealed together so that the display electrodes and data electrodes intersect with each other. A discharge gas is filled into an inside discharge space formed therebetween. In a panel structured as above, ultraviolet light is generated by gas discharge in each discharge cell. This ultraviolet light excites respective phosphors to emit R, G, or B color, for color display.

[0004] A general method of driving a panel is a so-called sub-field method: one field period is divided into a plurality of sub-fields and combination of light-emitting sub-fields provides gradation images for display. Now, each of the sub-fields has an initializing period, writing period, and sustaining period.

[0005] In the initializing period, all the discharge cells perform initializing discharge operation at a time to erase the history of wall electric charge previously formed in respective discharge cells and form wall electric charge necessary for the subsequent writing operation. Additionally, this initializing discharge operation serves to generate priming (priming for discharge = excited particles) for causing stable writing discharge.

[0006] In the writing period, scan pulses are sequentially applied to scan electrodes, and write pulses corresponding to the signals of an image to be displayed are applied to data electrodes. Thus, selective writing discharge is caused between scan electrodes and corresponding data electrodes for selective formation of wall electric charge.

[0007] In the subsequent sustaining period, a predetermined number of sustain pulses are applied between scan electrodes and corresponding sustain electrodes. Then, the discharge cells in which wall electric charge are formed by the writing discharge are selectively discharged and light is emitted from the discharge cells.

[0008] In this manner, to properly display an image, selective writing discharge must securely be performed in the writing period. However, there are many factors in increasing discharge delay in the writing discharge: restraints of the circuitry inhibit the use of high voltage for write pulses; and phosphor layers formed on the data electrodes make discharge difficult. For these reasons, priming for generating stable writing discharge is extremely important.

[0009] However, the priming caused by discharge rapidly decreases as time elapses. This causes the following problems in the method of driving a panel described above. In writing discharge occurring long time after the initializing discharge, priming generated in the initializing discharge is insufficient. This insufficient priming causes a large discharge delay and unstable wiring operation, thus degrading the image display quality. Additionally, when long wiring period is set for stable wiring operation, the time taken for the writing period is too long.

[0010] Proposed to address these problems are a panel and method of driving the panel in which auxiliary discharge electrodes are provided and discharge delay is minimized using priming caused by auxiliary discharge (see Japanese Patent Unexamined Publication No. 2002-297091, for example).

[0011] However, such panels have the following problems. Because the discharge delay of the auxiliary discharge itself is large, the discharge delay of the writing discharge cannot sufficiently be shortened. Additionally, because the operating margin of the auxiliary discharge is small, incorrect discharge may be induced in some panels.

[0012] Further, when the number of scan electrodes is increased for higher definition without shortening the discharge delay in the writing discharge sufficiently, the time taken for the writing period is too long and the time taken for the sustaining period is insufficient. As a result, luminance decreases. Additionally, increasing the partial pressure of xenon to increase the luminance and efficiency further increases the discharge delay and makes the writing operation unstable.

[0013] The present invention addresses these problems and aims to provide a method of driving a plasma display panel capable of performing stable and high-

speed writing operation.

DISCLOSURE OF THE INVENTION

[0014] To address these problems, the method of driving a plasma display panel of the present invention is a method of driving a plasma display panel having priming electrodes, in which priming discharge is generated prior to scanning of respective scan electrodes, in a wiring period of a sub-field.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015]

Fig: 1 is a sectional view showing an example of a panel used for a first exemplary embodiment of the present invention.

Fig. 2 is a schematic perspective view showing a structure of a rear substrate side of the panel.

Fig. 3 is a diagram showing an arrangement of electrodes in the panel.

Fig. 4 is a diagram showing a driving waveform in a method of driving the panel.

Fig. 5 is a diagram showing another driving waveform in a method of driving the panel.

Fig. 6 is a diagram showing still another driving waveform in a method of driving the panel.

Fig. 7 is a graph showing a relation between time elapsing from priming discharge and discharge delay.

Fig. 8 is a sectional view showing an example of a panel used for a second exemplary embodiment of the present invention.

Fig. 9 is a diagram showing an arrangement of electrodes in the panel.

Fig. 10 is a diagram showing a driving waveform in a method of driving the panel.

Fig. 11 is a diagram showing another driving waveform in a method of driving the panel.

Fig. 12 is diagram showing an example of a circuit block of a driver for implementing the methods of driving the panels used for first and second exemplary embodiments.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0016] Methods of driving plasma display panels in accordance with exemplary embodiments of the present invention are described hereinafter with reference to the accompanying drawings.

First Exemplary Embodiment

[0017] Fig. 1 is a sectional view showing an example of a panel used for the first exemplary embodiment of the present invention. Fig. 2 is a schematic perspective view showing the structure of the rear substrate side of the panel.

[0018] As shown in Fig. 1, front substrate 1 and rear substrate 2 both made of glass are faced with each other to sandwich a discharge space therebetween. In the discharge space, a mixed gas of neon and xenon for radiating ultraviolet light by discharge is filled.

[0019] On front substrate 1, a plurality of pairs of scan electrode 6 and sustain electrode 7 are formed in parallel with each other. Scan electrode 6 and sustain electrode 7 are made of transparent electrodes 6a and 7a, and metal buses 6b and 7b formed on transparent electrodes 6a and 7a, respectively. Now, between each scan electrode 6 and corresponding sustain electrode 7 on the side where metal buses 6b and 7b are formed, light-absorbing layer 8 made of a black material is provided. Projection 6b' of metal bus 6b in scan electrode 6 projects onto light-absorbing layer 8. Dielectric layer 4 and protective layer 5 are formed to cover these scan electrodes 6, sustain electrodes 7, and light-absorbing layers 8.

[0020] On rear substrate 2, a plurality of data electrodes 9 is formed in parallel with each other. Dielectric layer 15 is formed to cover these data electrodes 9. Further on the dielectric layer, barrier ribs 10 for partitioning the discharge space into discharge cells 11 are formed. As shown in Fig. 2, each barrier rib 10 is made of vertical walls 10a extending in parallel with data electrodes 9, and horizontal walls 10b for forming discharge cells 11 and forming clearance 13 between discharge cells 11. In each clearance 13, priming electrode 14 is formed in the direction orthogonal to data electrodes 9, to form priming space 13a. On the surface of dielectric layer 15 corresponding to discharge cells 11 partitioned by barrier ribs 10 and the side faces of barrier ribs 10, phosphor layers 12 are provided. However, no phosphor layer 12 is provided on the side of clearances 13.

[0021] When front substrate 1 is faced and sealed with rear substrate 2, each projection 6b' of metal bus 6b in scan electrode 6 formed on front substrate 1 that projects onto light-absorbing layer 8 is positioned in parallel with corresponding priming electrode 14 on rear substrate 2 and faced therewith to sandwich priming space 13a. In other words, the panel shown in Figs. 1 and 2 is structured to perform priming discharge between projections 6b' formed on the side of front substrate 1 and priming electrodes 14 formed on the side of rear substrate 2.

[0022] In Figs. 1 and 2, dielectric layer 16 is further formed to cover priming electrodes 14; however, this dielectric layer 16 need not be formed necessarily.

[0023] Fig. 3 is a diagram showing an arrangement of electrodes in the panel used for the first exemplary embodiment of the present invention. M columns of data electrodes D_1 to D_m (data electrodes 9 in Fig. 1) are arranged in the column direction. N rows of scan electrodes SC_1 to SC_n (scan electrodes 6 in Fig. 1), and n rows of sustain electrodes SU_1 to SU_n (sustain elec-

trodes 7 in Fig. 1) are alternately arranged in the row direction. Further, n rows of priming electrodes PR_1 to PR_n are arranged to be faced with the projections in scan electrodes SC_1 to SC_n. Thus, m × n discharge cells C_{ij} (discharge cells 11 in Fig. 1), each including a pair of scan electrode SC_i and sustain electrode SU_i (i = 1 to n) and one data electrode Dj (j = 1 to m), are formed in the discharge space. In clearances 13, n rows of priming spaces PS_i (priming space 13a in Fig. 1), each including the projection of scan electrode SC_i and priming electrode PR_i, are formed.

[0024] Next, a driving waveform for driving the panel and timing of the driving waveform are described.

[0025] Fig. 4 is a diagram showing a driving waveform in the method of driving the panel used for the first exemplary embodiment of the present invention. In this embodiment, one field period is made of a plurality of sub-fields, each including an initializing period, writing period, and sustaining period. Because the same operation is performed in each sub-field, except for the number of sustain pulses in the sustaining period, operation in one sub-filed is described hereinafter.

[0026] In the former half of the initializing period, each of data electrodes D_1 to D_m, sustain electrode SU_1 to SU_n, and priming electrodes PR_1 to PR_n is held at 0 (V). Applied to each of scan electrodes SC_1 to SC_n is a ramp waveform voltage gradually increasing from a voltage of V_{i1} not larger than discharge-starting voltage across the scan electrodes and sustain electrodes SU_1 to SU_n to a voltage of V_{i2} exceeding the discharge-starting voltage. While the ramp waveform voltage increases, first weak initializing discharge occurs between scan electrodes SC_1 to SC_n, and sustain electrodes SU_1 to SU_n, data electrodes D_1 to D_m, and priming electrodes PR_1 to PR_n. Thus, negative wall voltage accumulates on scan electrodes SC_1 to SC_n, and positive wall voltage accumulates on data electrodes D_1 to D_m, sustain electrodes SU_1 to SU_n, and priming electrodes PR_1 to PR_n. Now, the wall voltage on the electrodes is the voltage generated by the wall charge accumulating on the dielectric layers covering the electrodes.

[0027] In the latter half of the initializing period, each of sustain electrode SU_1 to SU_n is held at a positive voltage of Ve. Applied to each of scan electrodes SC_1 to SC_n is a ramp waveform voltage gradually decreasing from a voltage of V_{i3} not larger than discharge-starting voltage across the scan electrodes and sustain electrodes SU_1 to SU_n to a voltage of V_{i4} exceeding the discharge-starting voltage. During this application of the ramp voltage, second weak initializing discharge occurs between scan electrodes SC_1 to SC_n, and sustain electrodes SU_1 to SU_n, data electrodes D_1 to D_m, and priming electrodes PR_1 to PR_n. Then, the negative wall voltage on scan electrodes SC_1 to SC_n and the positive wall voltage on sustain electrodes SU_1 to SU_n are weakened. The positive wall voltage on data electrodes D_1 to D_m is adjusted to a value appropriate for writing operation. The positive wall voltage on priming electrodes PR_1 to PR_n is also adjusted to a value appropriate for priming operation. Thus, the initializing operation is completed.

[0028] In the writing period, scan electrodes SC_1 to SC_n are once held at a voltage of Vc. Then, a voltage of Vp is applied to priming electrode PR_1 of the first row. Especially in this case, voltage Vp is a high voltage sufficiently exceeding a voltage change (Vc - Vi_4) in scan electrodes SC_1 to SC_n. This causes priming discharge between priming electrode PR_1 and the projection of scan electrode SC_1, and the priming diffuses inside of discharge cells $C_{1,1}$ to $C_{1,m}$ in the first row corresponding to scan electrode SC_1 of the first row.

[0029] Next, scan pulse voltage Va is applied to scan electrode SC_1 of the first row, and positive write pulse voltage Vd is applied to data electrode D_k (k being an integer ranging from 1 to m) corresponding to the signal of an image to be displayed in the first row among data electrodes D_1 to D_k. At this time, discharge occurs at the intersection of data electrode Dk to which write pulse voltage Vd has been applied and scan electrode SC_1. This discharge develops to discharge between sustain electrode SU_1 and scan electrode SC_1 in corresponding discharge cell $C_{1,k}$. Then, positive wall voltage accumulates on scan electrode SC_1, and negative wall voltage accumulates on sustain electrode SU_1 in discharge cell $C_{1,k}$. Now, discharge occurs in discharge cell $C_{1,k}$ in the first row including scan electrode SC_1 of the first row with sufficient priming supplied from the priming discharge that has occurred between scan electrode SC_1 and priming electrode PR_1 immediately before the discharge. For this reason, discharge delay is extremely small, and thus high-speed and stable discharge occurs.

[0030] At the time of above writing operation in scan electrode SC_1 of the first row, voltage Vp is applied to priming electrode PR_2 corresponding to scan electrode SC_2 of the second row to cause priming discharge and diffuse the priming inside of discharge cells $C_{2,1}$ to $C_{2,m}$ in the second row corresponding to scan electrode SC_2 of the second row.

[0031] In a similar manner, writing discharge in the second row and priming discharge in the third row are performed. At this time, a series of writing discharge operations are performed with sufficient priming supplied from the priming discharge that has occurred immediately before the writing discharge operations. For this reason, the discharge delay is small and thus high-speed and stable discharge occurs.

[0032] Similar writing operations are performed in discharge cells including $C_{n,k}$, and the writing operation is completed.

[0033] In the sustaining period, after scan electrodes SC_1 to SC_n and sustain electrodes SU_1 to SU_n are reset to 0 (V) once, a positive sustain pulse voltage of Vs is applied to scan electrodes SC_1 to SC_n. At this time, in the voltage on scan electrode SC_i and sustain electrode SU_i in discharge cell $C_{i,j}$ in which writing discharge has

occurred, the wall voltage accumulating on scan electrode SC_i and sustain electrode SU_i is added to sustain pulse voltage Vs. For this reason, the voltage exceeds the discharge-starting voltage and sustain discharge occurs. In a similar manner, by alternately applying sustain pulses to scan electrodes SC_1 to SC_n and sustain electrodes SU_1 to SU_n, sustain discharge operations are successively performed in discharge cell $C_{i,j}$ in which the writing discharge has occurred, the number of times of sustain pulses.

[0034] As described above, unlike the writing discharge depending only on the priming in the initializing discharge in accordance with a conventional driving method, the writing discharge of the driving method in accordance with the present invention is performed with sufficient priming supplied from the priming discharge that has occurred immediately before the writing operation in respective discharge cells. This can achieve high-speed and stable writing discharge with a small discharge delay, and display a high-quality image.

[0035] Fig. 5 is a diagram showing another driving waveform in a method of driving the panel used for the first exemplary embodiment of the present invention. As shown in Fig. 5, in the writing period, voltage Vq not larger than the discharge-starting voltage (e.g. Vq = Vc - Vi_4) can commonly be applied to all the priming electrodes and the potential difference from voltage Vp, i.e. voltage Vp - Vq, can further be applied to the priming electrodes to be discharged, as a waveform applied to the priming electrodes. This case has an advantage of achieving a driver circuit using a driver IC with a low withstand voltage, because voltage Vp - Vq separately applied to each priming electrode for driving is low.

[0036] Fig. 6 is a diagram showing still another driving waveform in a method of driving a panel used for the first exemplary embodiment of the present invention. As shown in Fig. 6, to share a driver circuit and reduce the number of circuits, the timing of some priming pulses can be made the same. In Fig. 6, the timing of the priming pulses applied to priming electrodes PR_2, PR_3, and PR_4 are the same as the timing of the priming pulse applied to priming electrode PR_1. The timing of the priming pulses applied to priming electrodes PR_6, PR_7, and PR_8 are the same as the timing of the priming pulse applied to priming electrode PR_5. In this case, for discharge cells $C_{4,1}$ to $C_{4,m}$ in the forth row, for example, the priming discharge of priming electrode PR_4 is performed at the same timing as priming electrode PR_1. For this reason, although a curtain degree of time interval is provided from the priming discharge to the writing operation in discharge cells $C_{4,1}$ to $C_{4,m}$ in the fourth row, sufficient priming still remains after such a degree of time interval and thus writing can be performed with a small discharge delay. Fig. 7 is a graph showing the relation between the time elapsing from the priming discharge and the discharge delay. As shown in this graph, experiments show that writing operation can be performed with a small discharge delay when performed within 10 μs after the priming discharge.

Second Exemplary Embodiment

[0037] Fig. 8 is a sectional view showing an example of a panel used for the second exemplary embodiment of the present invention. Fig. 9 is a diagram showing an arrangement of electrodes in the panel. Same elements used in the first exemplary embodiment are denoted with the same reference marks and description thereof is omitted. In this embodiment, what is different from the first exemplary embodiment is that scan electrodes 6 and sustain electrodes 7 are alternately arranged in pairs like sustain electrode SU_1 - scan electrode SC_1 - scan electrode SC_2 - sustain electrode SU_2, etc. Therefore, priming electrode 14 is formed only in clearance 13 corresponding to the portion where a pair of scan electrodes 6 is adjacent to each other, to form priming space 13a. Consequently, while n rows of priming electrodes 14 are provided in corresponding clearances 13 in the first exemplary embodiment, n/2 rows of priming electrodes 14 are provided in every other one of clearances 13. Then, projection 6b' of metal bus 6b in only one of a pair of scan electrodes 6 is extended to the position corresponding to clearance 13 and formed on light-absorbing layer 8. In other words, priming discharge occurs between projection 6b' of metal bus 6b in one of adjacent scan electrodes 6 and priming electrode 14 formed on the side of rear substrate 2. In this embodiment, projections 6b' are provided only on odd-numbered scan electrodes SC_1, SC_3, etc. As described above, the panel used for the second exemplary embodiment is structured so that the priming space 13a of one row supplies priming to discharge cells in two rows.

[0038] Next, a driving waveform for driving the above panel and the timing thereof are described.

[0039] Fig. 10 is a diagram showing a driving waveform in the method of driving the panel used for the second exemplary embodiment of the present invention. Also in this embodiment, operation in one sub-field is described.

[0040] Because the operation in the initializing period is the same as that of the first exemplary embodiment, description thereof is omitted.

[0041] In the writing period, like the first exemplary embodiment, scan electrodes SC_1 to SC_n are held at voltage Vc once, and voltage Vp is applied to priming electrode PR_1 of the first row. Then, priming discharge occurs between priming electrode PR_1 and the projection of scan electrode SC_1. Thus, the priming diffuses inside of discharge cells $C_{1,1}$ to $C_{1,m}$ in the first row corresponding to scan electrode SC_1. The priming also diffuses inside of discharge cells $C_{2,1}$ to $C_{2,m}$ in the second row corresponding to scan electrode SC_2 at the same time.

[0042] Next, scan pulse voltage Va is applied to scan electrode SC_1 of the first row, and write pulse voltage Vd corresponding to video signals is applied to data

electrode D_k (k being an integer ranging from 1 to m), for writing operation on discharge cell $C_{1,k}$ in the first row.

[0043] Sequentially, scan pulse voltage Va is applied to scan electrode SC_2 of the second row, and write pulse voltage Vd corresponding to video signals is applied to data electrode D_k (k being an integer ranging from 1 to m), for writing operation in discharge cell $C_{2,k}$ in the second row. At this time, at the same time as the above writing operation using scan electrode SC_2 of the second row, voltage Vp is applied to priming electrode PR_3 corresponding to scan electrode SC_3 of the third row to cause priming discharge. Then the priming diffuses inside of discharge cells $C_{3,1}$ to $C_{3,m}$ in the third row corresponding to scan electrode SC_3 of the third row and discharge cells $C_{4,1}$ to $C_{4,}m$ in the fourth row corresponding to scan electrode SC_4 of the fourth row.

[0044] In the same manner, writing operations are sequentially performed. However, in the writing operation in odd-numbered discharge cells $C_{p,1}$ to $C_{p,m}$ (p = 1, 3, 5, etc.), no priming discharge is caused. In contrast, in the writing operation in even-numbered discharge cells $C_{q,1}$ to $C_{q,m}$ (q = 2, 4, 6, etc), priming discharge is caused in priming electrode PR_{q+1} corresponding to the (q+1)-th scan electrode SC_{q+1}, and the priming diffuses inside of discharge cells $C_{q+1,1}$ to $C_{q+1,m}$ in the (q+1)-th row and discharge cells $C_{q+2,1}$ to $C_{q+2,m}$ in the (q+2)-th row.

[0045] The similar writing operations are performed in the discharge cells including those in the n-th row, and the writing operations are completed.

[0046] The operation in the sustaining period is the same as that of the first exemplary embodiment, and thus the description thereof is omitted.

[0047] As described above, like the first exemplary embodiment, the writing discharge in the driving method of the present invention is performed with sufficient priming supplied from the priming discharge that has occurred immediately before the writing operation in respective discharge cells. For this reason, the discharge delay is small, and thus high-speed and stable discharge is possible.

[0048] Further, in the second exemplary embodiment, electrodes in the vicinity of priming spaces 13a are priming electrodes 14 and scan electrodes 6 only. This also gives an advantage of stable action of the priming discharge itself because the priming discharge is unlikely to cause other unnecessary discharge, e.g. incorrect discharge involving sustain electrodes 7.

[0049] Incidentally, as shown in Fig. 10, like the first exemplary embodiment, in the second exemplary embodiment, a voltage of Vq not larger than the discharge-starting voltage can commonly be applied to all the priming electrodes PR_1 to PR_n, and a voltage of Vp - Vq can be further applied to priming electrodes to be discharged, in the writing period.

[0050] Fig. 11 is a diagram showing another waveform in a method of driving the panel used for the second exemplary embodiment. As shown in the waveform, the timing of some priming pulses can be made the same. In Fig. 11, the timing of the priming pulse applied to priming electrode PR_3 is the same as the timing of the priming pulse applied to priming electrode PR_1. The timing of the priming pulse applied to priming electrode PR_7 is the same as the timing of the priming pulse applied to priming electrode PR_5. However, it is important to cause writing discharge within 10 μs after the priming discharge.

[0051] Incidentally, because respective electrodes of an AC type PDP are surrounded by the dielectric layers and insulated from the discharge space. For this reason, direct-current components make no contribution to discharge itself. Therefore, of course, even the use of waveforms in which direct-current components are added to the driving waveforms of the first or second exemplary embodiment can provide similar effects.

[0052] Fig. 12 is a diagram showing an example of a circuit block of a driver for implementing the methods of driving the panels used for the first and second exemplary embodiments. Driver 100 of the exemplary embodiments of the present invention includes: video signal processor circuit 101, data electrode driver circuit 102, timing controller circuit 103, scan electrode driver circuit 104 and sustain electrode driver circuit 105, and priming electrode driver circuit 106. A video signal and synchronizing signal are fed into video signal processor circuit 101. Responsive to the video signal and synchronizing signal, video signal processor circuit 101 outputs a sub-field signal for controlling whether or not to light each sub-field, to data electrode driver circuit 102. The synchronizing signal is also fed into timing controller circuit 103. Responsive to the synchronizing signal, timing controller circuit 103 outputs a timing control signal to data electrode driver circuit 102, scan electrode driver circuit 104, sustain electrode driver circuit 105, and priming electrode driver circuit 106.

[0053] Responsive to the sub-field signal and the timing control signal, data electrode driver circuit 102 applies a predetermined driving waveform to data electrodes 9 (data electrodes D_1 to D_m in Fig. 3) in the panel. Responsive to the timing control signal, scan electrode driver circuit 104 applies a predetermined driving waveform to scan electrodes 6 (scan electrodes SC_1 to SC_n in Fig. 3) in the panel. Responsive to the timing control signal, sustain electrode driver circuit 105 applies a predetermined driving waveform to sustain electrodes 7 (sustain electrodes SU_1 to SU_n in Fig. 3) in the panel. Responsive to the timing control signal, priming electrode driver circuit 106 applies a predetermined driving waveform to priming electrodes 14 (priming electrodes PR_1 to PR_n in Fig. 3) in the panel. Necessary electric power is supplied to data electrode driver circuit 102, scan electrode driver circuit 104, sustain electrode driver circuit 105, and priming electrode driver circuit 106 from a power supply circuit.

[0054] The above circuit block can constitute a driver for implementing the methods of driving the panels of

the exemplary embodiments of the present invention.

[0055] As described above, the present invention can provide a method of driving a plasma display panel capable of performing stable and high-speed writing operation.

INDUSTRIAL APPLICABILITY

[0056] The method of driving a plasma display panel of the present invention can perform stable and high-speed writing operation. Thus, the present invention is useful as a method of driving an AC type plasma display panel.

Reference marks in the drawings

[0057]

1	Front substrate
2	Rear substrate
4	Dielectric layer
5	Protective layer
6	Scan electrode
6a, 7a	Transparent electrode
6b, 7b	Metal bus
6b'	Projection
7	Sustain electrode
8	Light-absorbing layer
9	Data electrode
10	Barrier rib
10a	Vertical wall
10b	Horizontal wall
11	Discharge cell
12	Phosphor layer
13	Clearance
13a	Priming space
14	Priming electrode
100	Driver
101	Video signal processor circuit
102	Data electrode driver circuit
103	Timing controller circuit
104	Scan electrode driver circuit
105	Sustain electrode driver circuit
106	Priming electrode driver circuit

Claims

1. A method of driving a plasma display panel comprising a plurality of scan electrodes and sustain electrodes arranged in parallel with each other, and a plurality of data electrodes arranged in a direction intersecting the scan electrodes, in which one field period is made of a plurality of sub-fields, each including an initializing period, writing period, and sustaining period, the method comprising:

   providing a plurality of priming electrodes in parallel with the scan electrodes, the priming electrodes generating priming discharge between the priming electrodes and the corresponding scan electrodes; and

   prior to scanning of the scan electrodes corresponding respective priming electrodes, applying, to the respective priming electrodes, voltage for causing priming discharge between the priming electrodes and the corresponding scan electrodes, in the writing period of each of the sub-fields.

2. The method of driving a plasma display panel of claim 1, wherein a time interval between application of the voltage to the priming electrodes for causing the priming discharge and the scanning of the corresponding scan electrodes is within 10 μs, in the writing period of the sub-fields.

FIG. 1

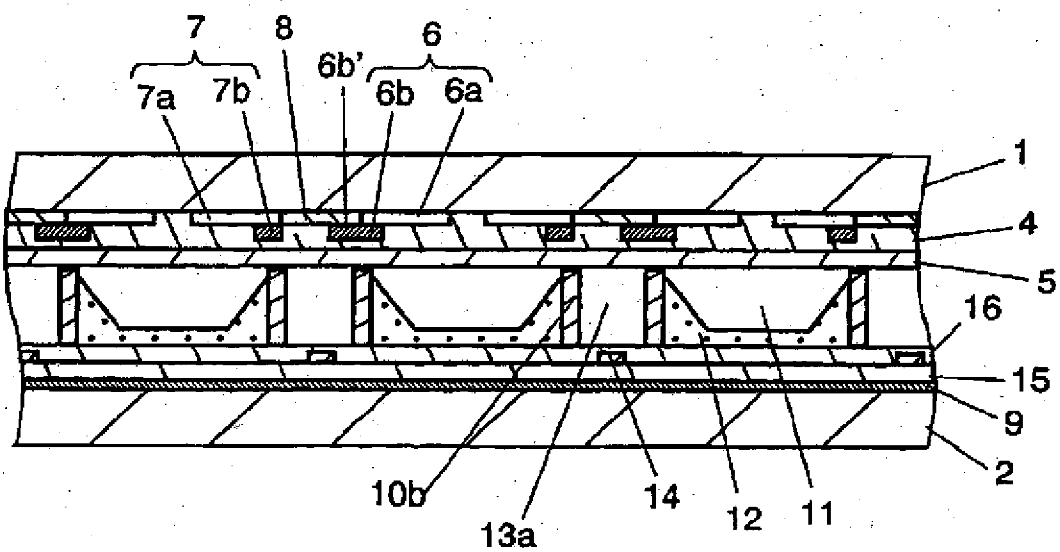

7
8
6
6b'
7a
7b
6b
6a
1
4
5
16
15
9
2
10b
13a
14
12
11

FIG. 2

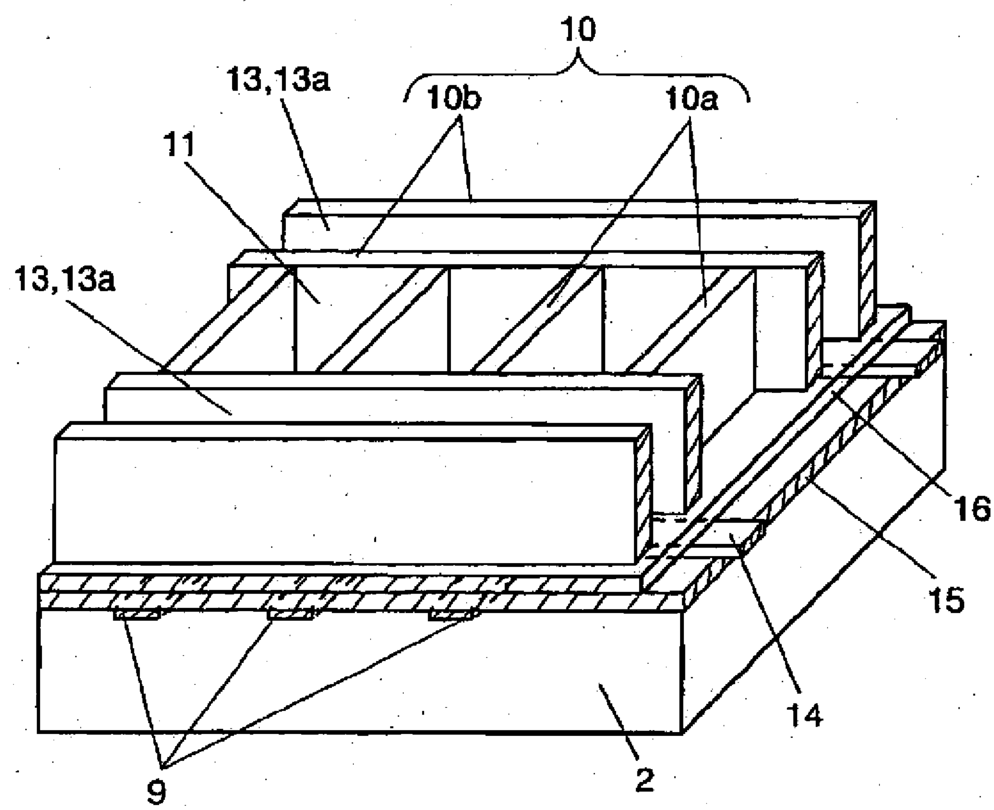

10
13,13a
10b
10a
11
13,13a
16
15
14
9
2

FIG. 3

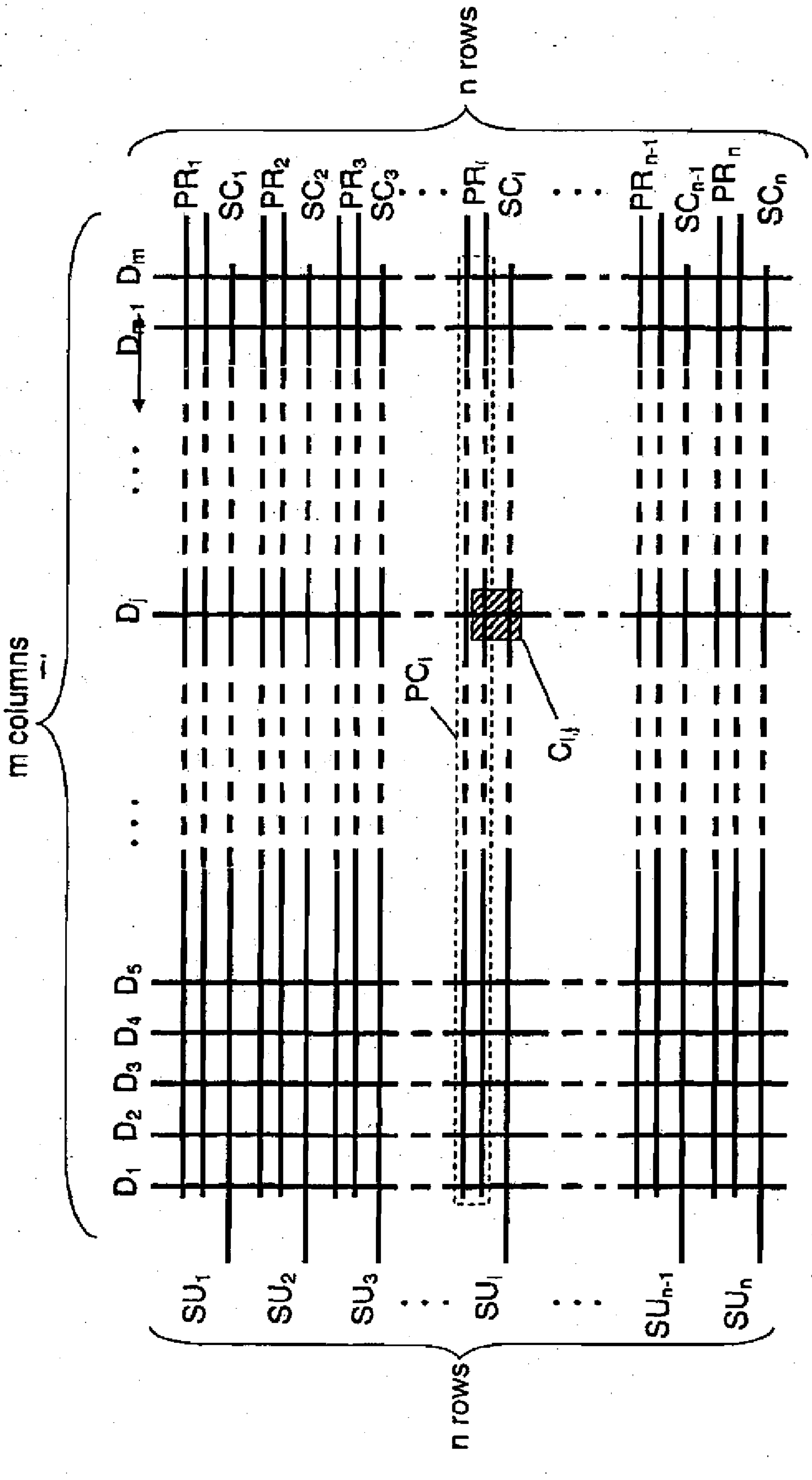

m columns
n rows
n rows
D_1 D_2 D_3 D_4 D_5 D_j D_{m-1} D_m
PR_1 SC_1 PR_2 SC_2 PR_3 SC_3 PR_i SC_i PR_{n-1} SC_{n-1} PR_n SC_n
SU_1 SU_2 SU_3 SU_i SU_{n-1} SU_n
PC_i
$C_{i,j}$

FIG. 4

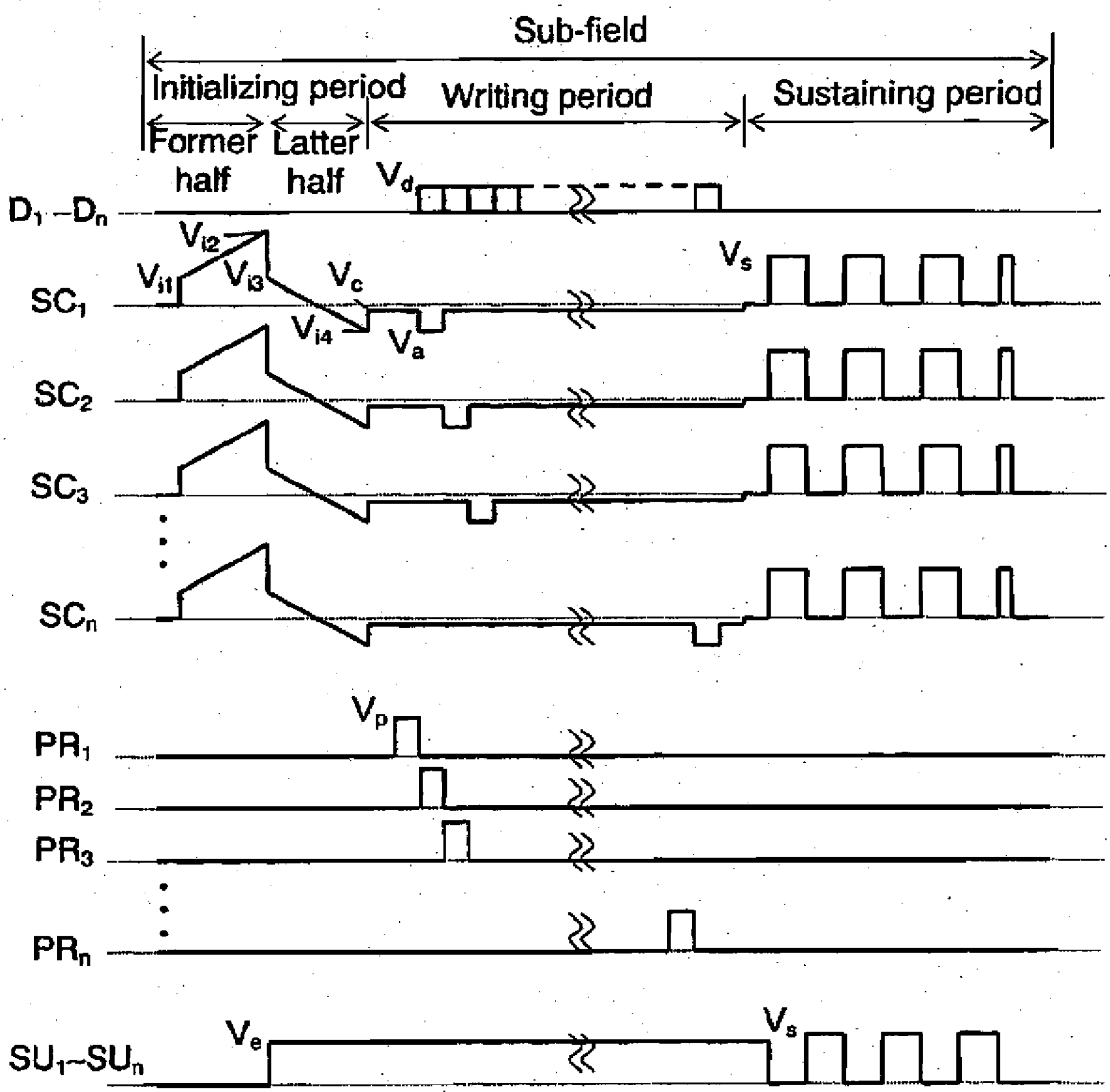

Sub-field
Initializing period
Writing period
Sustaining period
Former half
Latter half
D1 - Dn
Vd
SC1
SC2
SC3
SCn
Vi1
Vi2
Vi3
Vi4
Vc
Va
Vs
PR1
PR2
PR3
PRn
Vp
SU1~SUn
Ve
Vs

FIG. 5

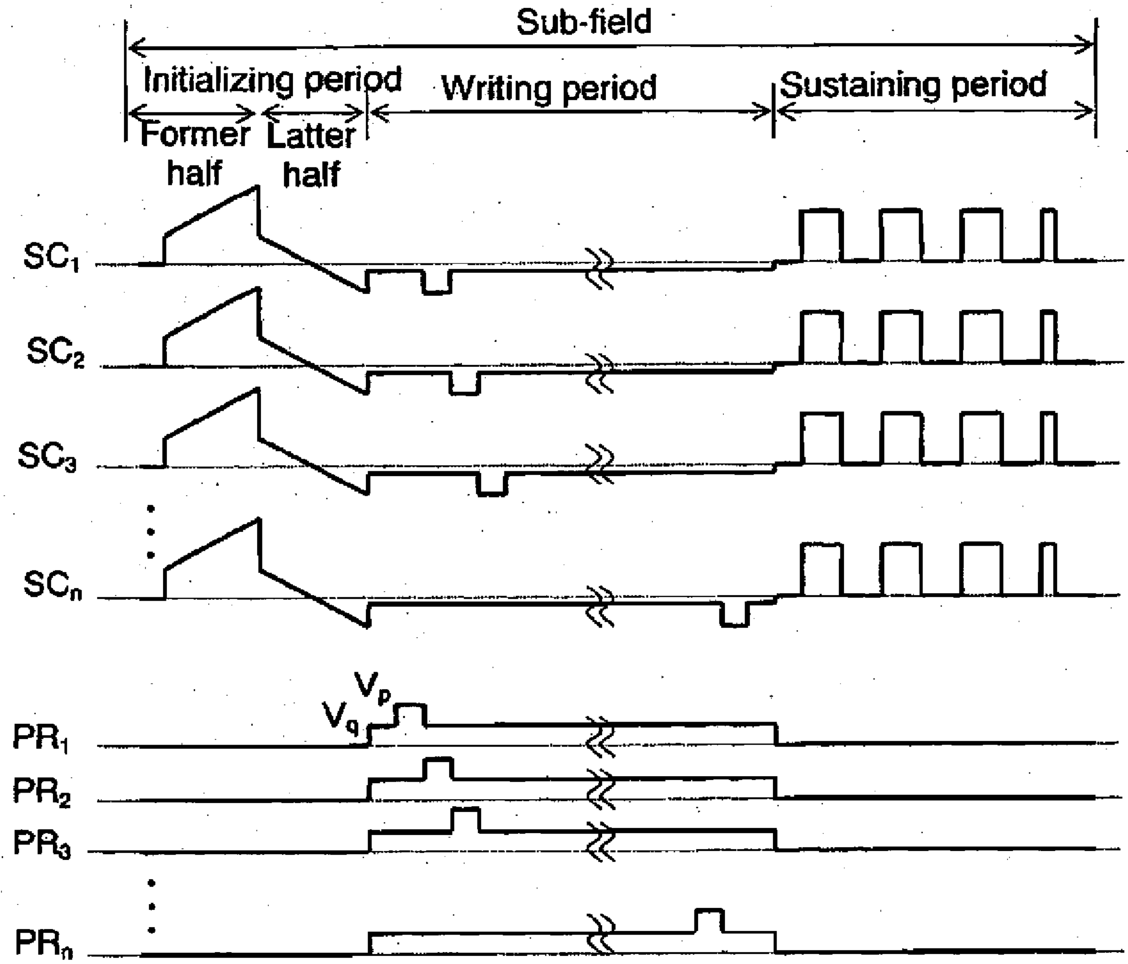

Sub-field
Initializing period
Writing period
Sustaining period
Former half
Latter half
SC1
SC2
SC3
SCn
Vp
Vq
PR1
PR2
PR3
PRn

FIG. 6

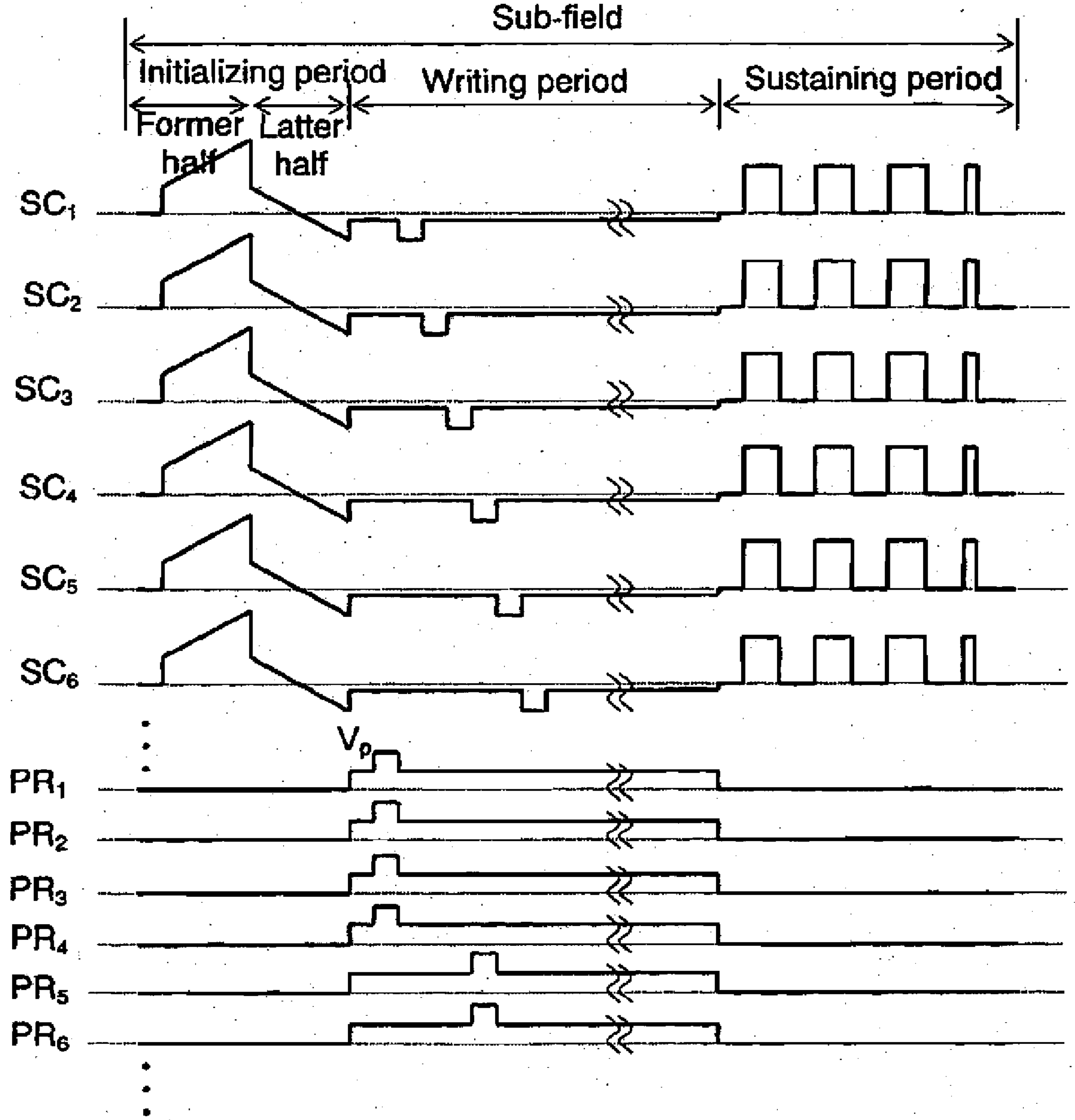

Sub-field
Initializing period
Writing period
Sustaining period
Former half
Latter half
SC1
SC2
SC3
SC4
SC5
SC6
Vp
PR1
PR2
PR3
PR4
PR5
PR6

FIG. 7

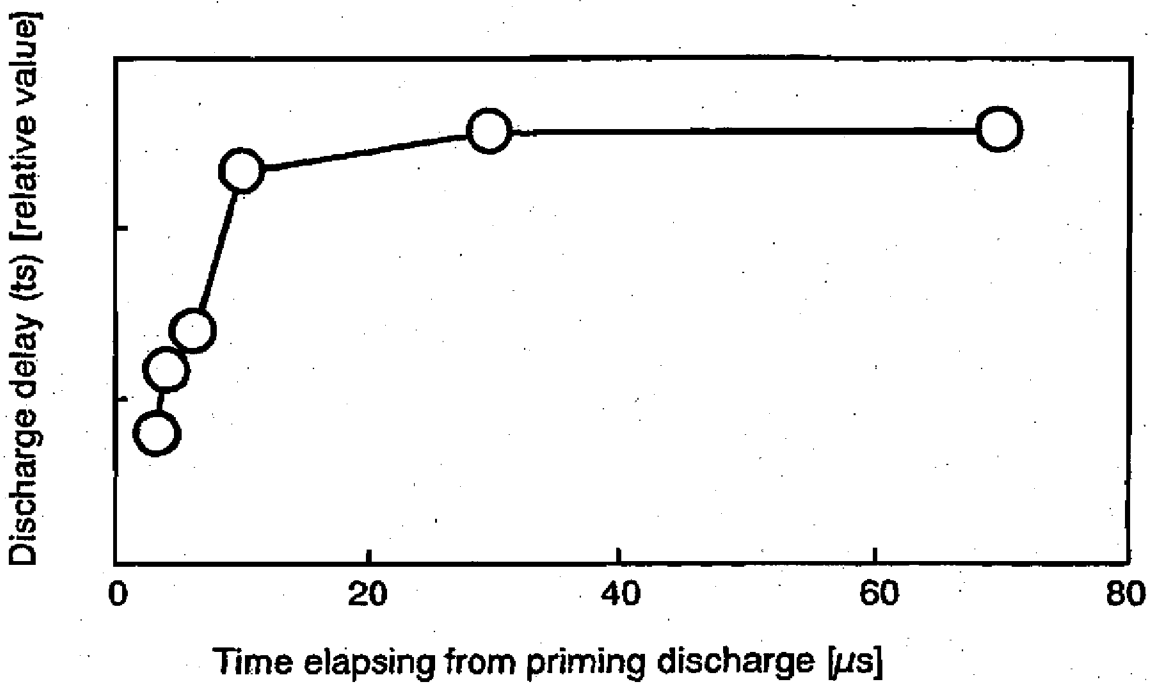

Discharge delay (ts) [relative value]
0
20
40
60
80
Time elapsing from priming discharge [μs]

FIG. 8

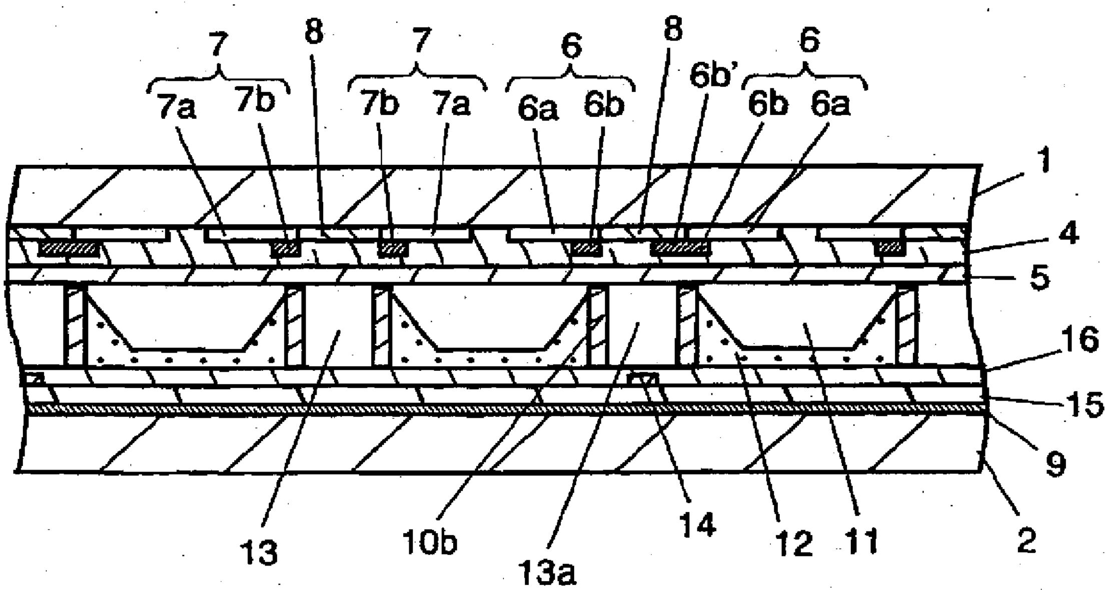

7
8
7
6
8
6
7a
7b
7b
7a
6a
6b
6b'
6b
6a
1
4
5
16
15
9
2
13
10b
13a
14
12
11

FIG. 9

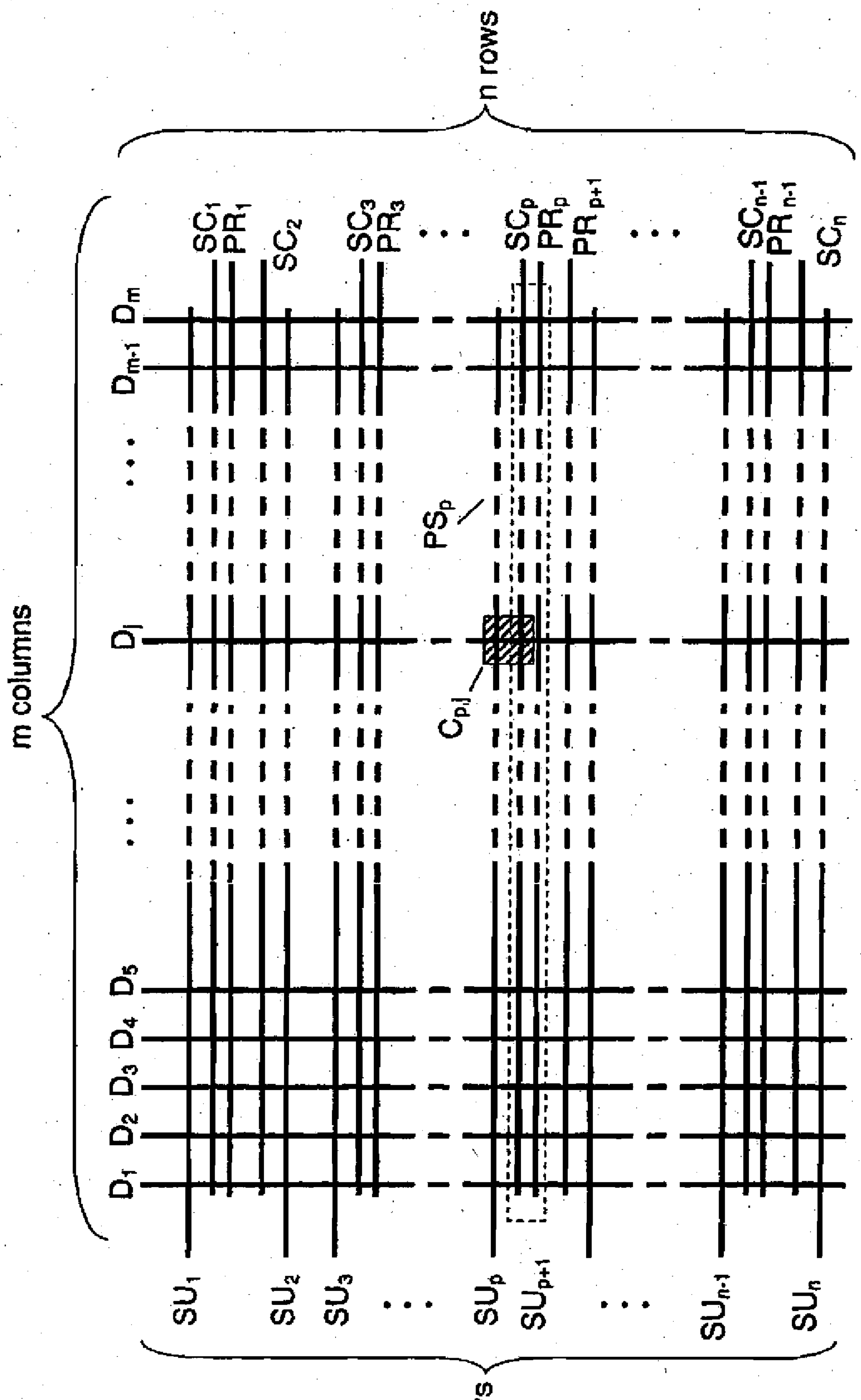

m columns
n rows
n rows
D_1 D_2 D_3 D_4 D_5 D_j D_{m-1} D_m
SU_1 SU_2 SU_3 SU_p SU_{p+1} SU_{n-1} SU_n
SC_1 PR_1 SC_2 SC_3 PR_3 SC_p PR_p PR_{p+1} SC_{n-1} PR_{n-1} SC_n
PS_p
$C_{p,j}$

FIG. 10

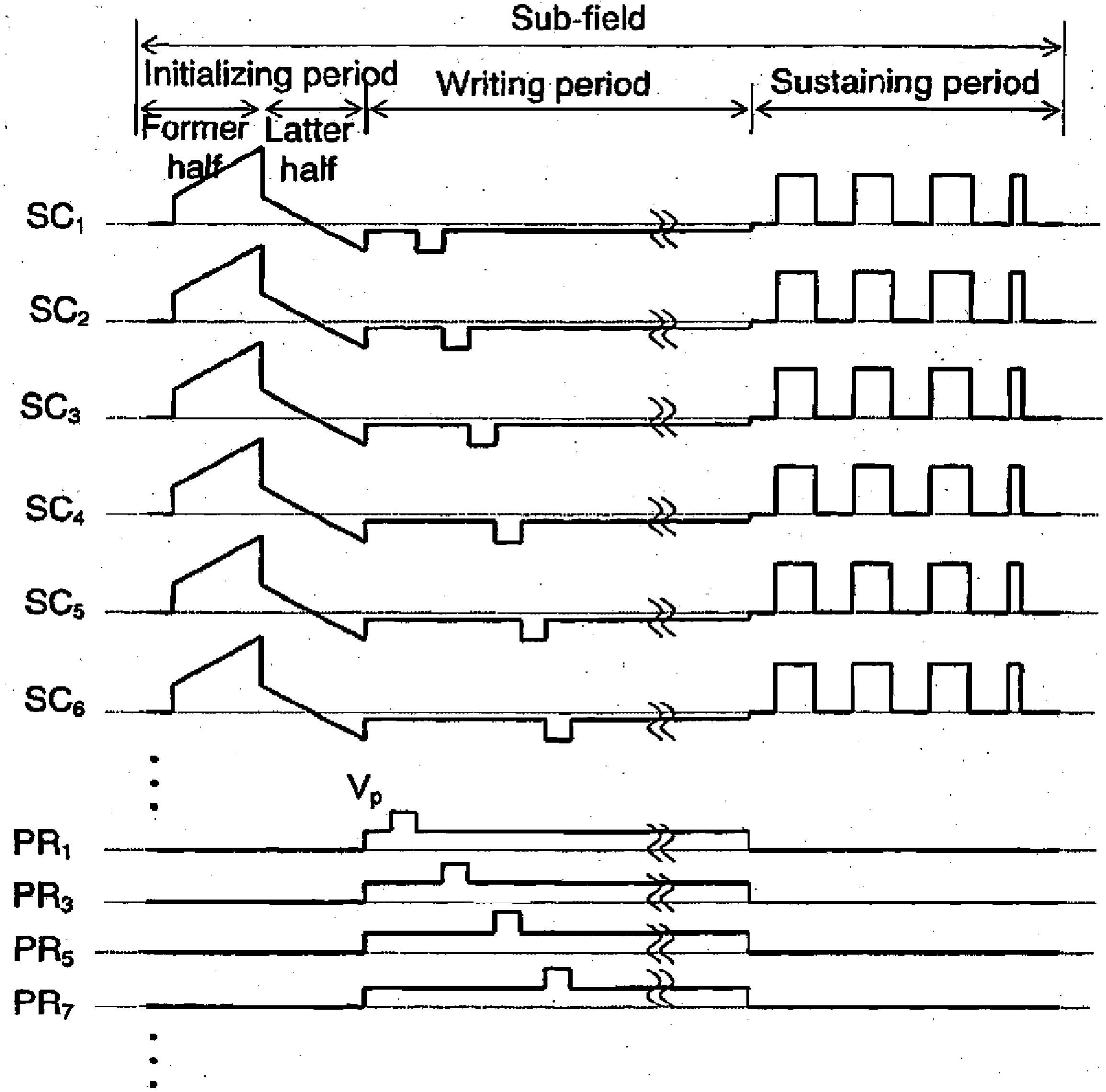

Sub-field
Initializing period
Writing period
Sustaining period
Former half
Latter half
SC1
SC2
SC3
SC4
SC5
SC6
Vp
PR1
PR3
PR5
PR7

FIG. 11

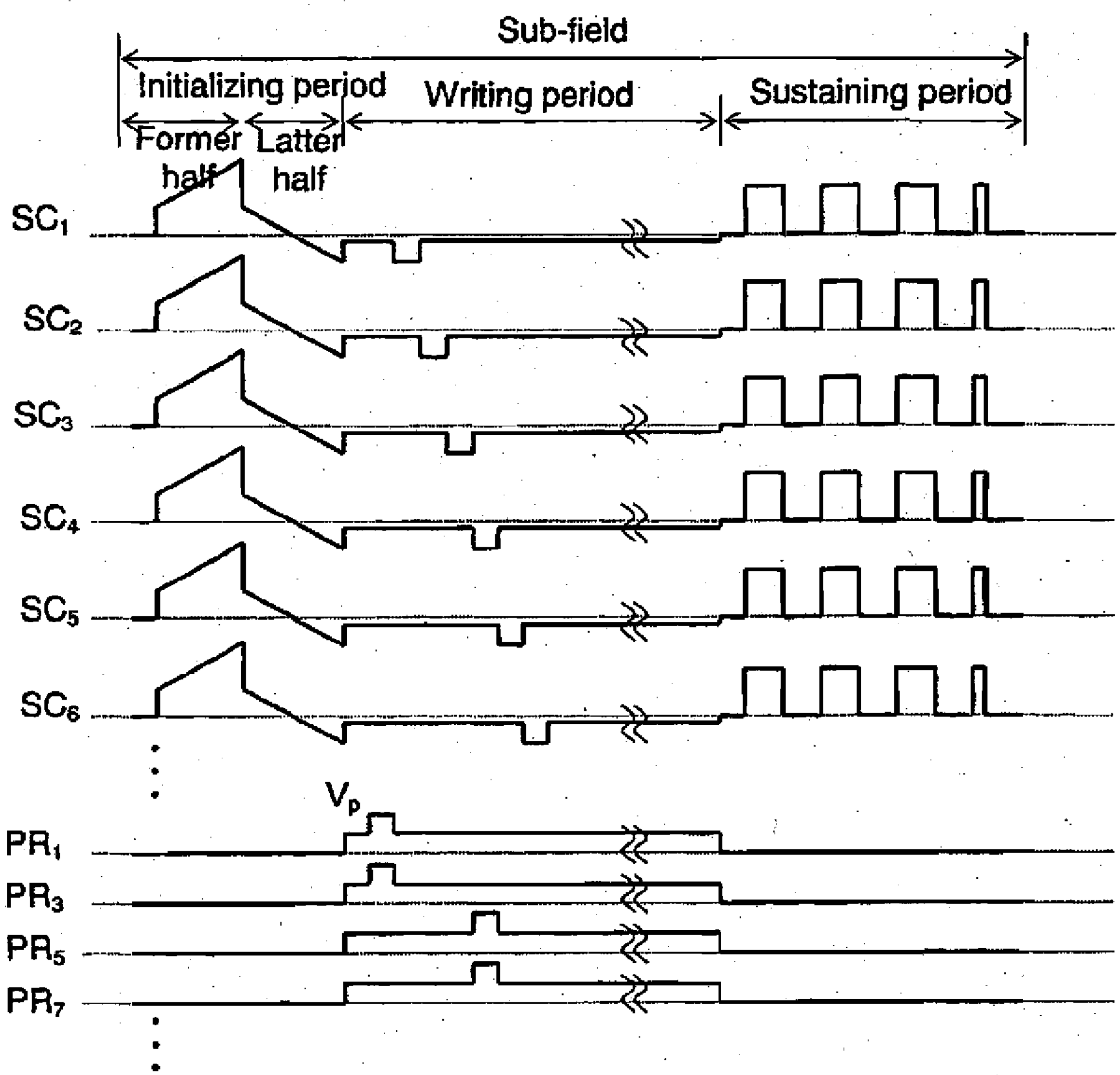
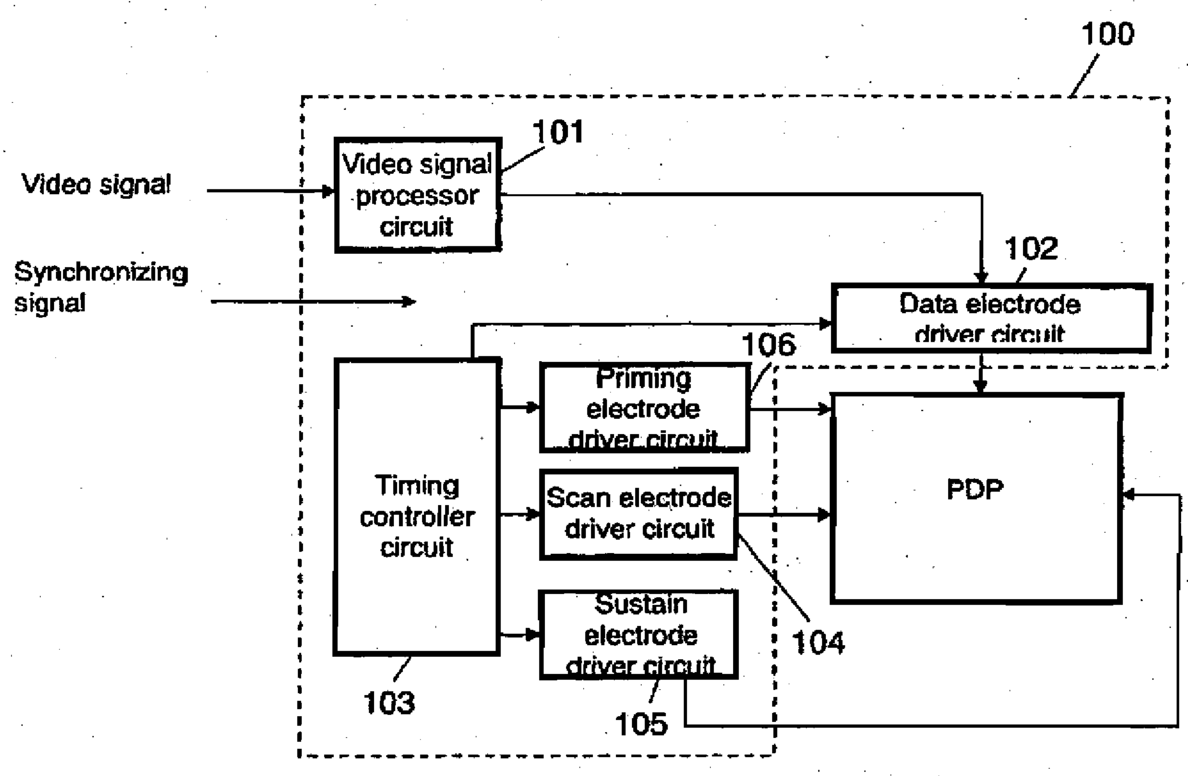

Sub-field
Initializing period
Writing period
Sustaining period
Former half
Latter half
SC1
SC2
SC3
SC4
SC5
SC6
Vp
PR1
PR3
PR5
PR7

FIG. 12


100
101
Video signal
Video signal processor circuit
Synchronizing signal
102
Data electrode driver circuit
106
Priming electrode driver circuit
Timing controller circuit
Scan electrode driver circuit
PDP
Sustain electrode driver circuit
104
103
105

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2004/003950

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] G09G3/28, G09G3/20, H01J11/00-02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] G09G3/28, G09G3/20, H01J11/00-02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1926-1996	Toroku Jitsuyo Shinan Koho	1994-2004
Kokai Jitsuyo Shinan Koho	1971-2004	Jitsuyo Shinan Toroku Koho	1996-2004

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2001-185034 A (LG Electronics Inc.), 06 July, 2001 (06.07.01), Par. Nos. [0026] to [0034]; Figs. 5 to 7 & KR 2001038965 A	1-2
	JP 8-96714 A (NEC Corp.), 12 April, 1996 (12.04.96),	
X	Par. Nos. [0039] to [0046]; Figs. 1 to 3	1
Y	Par. Nos. [0039] to [0046]; Figs. 1 to 3 (Family: none)	2
Y	JP 9-245627 A (Mitsubishi Electric Corp.), 19 September, 1997 (19.09.97), Par. No. [0065]; Fig. 19 (Family: none)	2

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents:
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"P" document published prior to the international filing date but later than the priority date claimed
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search 21 June, 2004 (21.06.04)	Date of mailing of the international search report 06 July, 2004 (06.07.04)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2004/003950

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 11-297211 A (NEC Corp.), 29 October, 1999 (29.10.99), Par. Nos. [0028] to [0045]; Figs. 1 to 8 & KR 99083169 A & US 2001/020924 A1	1-2
A	JP 11-144626 A (NEC Corp.), 28 May, 1999 (28.05.99), Par. Nos. [0025] to [0059]; Figs. 1 to 10 (Family: none)	1-2